IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): [[The]] A video signal processing circuit ~~of claim 1~~, comprising:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control unit,

wherein said pixel data corresponding to said pixels representing said scanning line stored in said latch circuit is displayed on said display screen,

in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control unit delays for a predetermined delay time reading of said pixel data corresponding to said pixels representing said scanning line and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again, and

~~wherein~~ said control unit comprises a delay unit which delays and inputs a display read control signal and a data latch signal for said predetermined delay time during a period which is after a point at which said memory clock signal corresponding to writing of said pixel data in said GRAM is supplied, said writing accompanying said contention, but which

is before supplying of the next memory clock signal following said memory clock signal so that said latch circuit reads pixel data corresponding to pixels representing said scanning line.

Claim 3 (Previously Presented): The video signal processing circuit of claim 2, wherein said predetermined delay time can be adjusted in a variable manner.

Claim 4 (Currently Amended): The video signal processing circuit of claim [[1]] 2, wherein said control unit comprises a monitoring unit which monitors whether writing of said pixel data in said GRAM contends against reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM.

Claim 5 (Previously Presented): The video signal processing circuit of claim 4, wherein said control unit comprises a delay unit which delays reading of said pixel data corresponding to said pixels representing said scanning line based on a monitoring result obtained by said monitoring unit and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

Claim 6 (Currently Amended): [[The]] A video signal processing circuit ~~of claim 1~~, comprising:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control unit,

wherein said pixel data corresponding to said pixels representing said scanning line stored in said latch circuit is displayed on said display screen,

in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control unit delays for a predetermined delay time reading of said pixel data corresponding to said pixels representing said scanning line and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again, and

~~wherein~~ when writing of said pixel data in said GRAM is executed plural times during a contention-free memory update period in which said pixel data corresponding to said pixels representing said scanning line are read to said latch circuit from said GRAM said control unit upon occurrence of said contention delays reading of said pixel data corresponding to said pixels representing said scanning line between a period of writing said pixel data and a period of writing next pixel data, and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM again plural times during said contention-free memory update period.

Claims 7-8 (Canceled).